

Summarized Instruction Repertory

This section is planned as a condensed description of the Orion Instruction Repertory, for quick reference. It is taken from the digitised version of the ORION Programming Manual prepared by Dr Malcolm Bigg, one of ORION 2 's designers and to be found at :

<http://malcolm.bigg.me.uk/Orion>

First we give an overview of the ORION instruction set, in a reproduction of the original two-sided Ferranti summary sheet. For a full description of the detailed effects of the various instructions and their times see section 3 of the ORION Programming Manual quoted above.

The instruction sheets are followed by a description of ORION pseudo-registers, taken from (see attached GIF file Order codes 2 }

<p>00 $z' = x + y$ 01 $z' = x - y$ 02 $z' = y - x$ 03 $z' = -y$ 04 $z' = y$ 05 $z' = x \& y$ 06 $z' = x \vee y$ 07 $z' = x \neq y$</p>	<p>10 $z' = x + Y$ 11 $z' = x - Y$ 12 $z' = Y - x$ 13 $z' = -Y$ 14 $z' = Y$ 15 $z' = x \& Y$ 16 $z' = x \vee Y$ 17 $z' = x \neq Y$</p>	<p>20 $z' = x + \phi Y$ 21 $z' = x - \phi Y$ 22 $z' = \phi Y - x$ 23 $z' = -\phi Y$ 24 $z' = \phi Y$ 25 $z' = x \& \phi Y$ 26 $z' = x \vee \phi Y$ 27 $z' = x \neq \phi Y$</p>	<p>30 $z'_1 = x_1 Y_1$ 31 $z'_2 = (x_2 Y_2) r$ 32 $z'_3 = x_3 Y_3$ 33 $z'_4 = z'_3 + x_4 Y_4$ 34 $z'_5 = x_5 Y_5$ 35 Unassigned; 36 illegal 37 illegal</p>	<p>40* Unrounded: integral quotient to Z, remainder to Z + 1 41* Rounded: rounded integral quotient to Z 42* Rounded with d.l. mid-point quotient: integral part to Z, fractional part to Z + 1 43* Rounded: fractional quotient to Z 44* Unrounded with d.l. dividend: integral quotient to Z, remainder to Z + 1 45* Rounded with d.l. dividend: fractional quotient to Z 46 Unassigned; illegal. 47 Unassigned; illegal.</p>					
<p>50 $z' = x \cdot 2^Y$ 51 $z' = x \cdot 2^{-Y}$ 52 $z' = x$ up Y bits 53 $z' = x$ down Y bits 54 $z'_1 = x \cdot 2^Y$ 55 $z'_2 = x \cdot 2^{-Y}$ 56 $z'_L = x \cdot L$ up Y bits 57 $z'_L = x \cdot L$ down Y bits</p> <p>See other side for note on timing.</p>		<p>60 $y = z$ 61 $y \neq z$ 62 $y > z$ ($z < y$) 63 $y \neq z$ ($z > y$) 64 $y < z$ ($z > y$) 65 $y \neq z$ ($z \leq y$) 66 $\phi Y = z$ 67 $\phi Y \neq z$</p> <p>For 2-address, put $z = 0$</p>		<p>70 $Y = z_m$ 71 $Y \neq z_m$ 72 $Y > z_m$ ($z_m < Y$) 73 $Y \neq z_m$ ($z_m > Y$) 74 $Y < z_m$ ($z_m \geq Y$) 75 $Y \neq z_m$ ($z_m \leq Y$) 76 $\bar{Y} \& z = 0$ 77 $\bar{Y} \& z \neq 0$</p> <p>For 2-address, put $z = 0$ (not 76, 77)</p>		<p>80 $z' = z + 1$ Jump to X if: 81 $z' = z + 1$ to $z'_m \neq Y$ 82 $z' = z - 1$ to $z'_m = Y$ 83 $z' = z - 1$ if $z'_m \neq Y$ 84 Jump to X if in Y 85 if char. Z is not in Y 86 $z'_m = c + 1, z'_s = OVR$ Enter if char. SP is not in Y 87 $OVR' = 0$, jump to X S/R OVR' = OVR $\vee z_2$ Leave S/R OVR' = OVR $\vee Y_5$ Jump to X + Y_m</p>		<p>90 $z'_g = x_g + Y_g$ 91 $z'_g = x_g - Y_g$ 92 $z'_g = Y_g - x_g$ 93 $z'_g = -Y_g$ 94 $z'_g = x_g \cdot Y_g$ 95 $z'_g = x_g / Y_g$ 96 Unassigned; illegal. 97 $z'_1 =$ no. of places to standardize $x_g - Y_g$</p>	
<p>100* Convert characters to binary 101* Convert binary to characters 102* $z'_g = (x_p + v) \cdot 2^Y$, Y signed 103 $z'_p = x_g \cdot 2^Y$, Y signed 104* Convert card 2-character data 105 Unassigned; illegal. 106 Unassigned; illegal. 107 Unassigned; illegal.</p>		<p>110 $x' = (x \& \bar{y}) \vee (x \& y)$ wherever mask 111 $x' = (x \& \bar{y}) \vee (x \& Y)$ (Y, Y or ϕY) 112 $x' = (x \& \phi Y) \vee (z \& \phi Y)$ has 1-bits. 113 Unassigned; illegal 114 (3) $z' = y, y' = x$ (2) $x' = y, y' = x$ (exchange) 115 Add l.s. 6 bits of Y to m.s. 6 bits of X; add rest of Y to x_m: end-around carry 116 Add X and Y to corresponding before any replacements Modify next instruction 117 addresses in next instruction after therein</p>		<p>120* Count 1-bits 121* Cyclic shift 122* Table look-up 123* Insert (append) field 124* Find end-most 1-bit 125* Standardize unpacked floating-point number 126* Justify d.l. number 127 to 137 Unassigned; illegal.</p>		<p>140. N 0 DEVICE Peripheral 142 FROM LENGTH Transfer Modes on other 141. N 0 DRUMADDR Drum 142 COREADDR LENGTH Transfer side 142 TO 0 Internal 142 FROM LENGTH Transfer 143 (3) Copy z into X to X + Y - 1 (2) Clear to zero X to X + Y - 1 144 Search table $\left[\begin{matrix} w \geq y \text{ (ascending)} \\ w \leq y \text{ (descending)} \end{matrix} \right]$ 145 starting at X $\left[\begin{matrix} w \geq y \\ w \leq y \end{matrix} \right]$ 146 for first $\left[\begin{matrix} w_u = Y_u \text{ or } w_m = 0 \\ \text{and set } z' = \text{address of } w \end{matrix} \right]$ 147 Unassigned; illegal.</p>		<p>140. N 0 DEVICE Peripheral 142 FROM LENGTH Transfer Modes on other 141. N 0 DRUMADDR Drum 142 COREADDR LENGTH Transfer side 142 TO 0 Internal 142 FROM LENGTH Transfer 143 (3) Copy z into X to X + Y - 1 (2) Clear to zero X to X + Y - 1 144 Search table $\left[\begin{matrix} w \geq y \text{ (ascending)} \\ w \leq y \text{ (descending)} \end{matrix} \right]$ 145 starting at X $\left[\begin{matrix} w \geq y \\ w \leq y \end{matrix} \right]$ 146 for first $\left[\begin{matrix} w_u = Y_u \text{ or } w_m = 0 \\ \text{and set } z' = \text{address of } w \end{matrix} \right]$ 147 Unassigned; illegal.</p>	
<p>140. N 0 DEVICE Peripheral 142 FROM LENGTH Transfer Modes on other 141. N 0 DRUMADDR Drum 142 COREADDR LENGTH Transfer side 142 TO 0 Internal 142 FROM LENGTH Transfer 143 (3) Copy z into X to X + Y - 1 (2) Clear to zero X to X + Y - 1 144 Search table $\left[\begin{matrix} w \geq y \text{ (ascending)} \\ w \leq y \text{ (descending)} \end{matrix} \right]$ 145 starting at X $\left[\begin{matrix} w \geq y \\ w \leq y \end{matrix} \right]$ 146 for first $\left[\begin{matrix} w_u = Y_u \text{ or } w_m = 0 \\ \text{and set } z' = \text{address of } w \end{matrix} \right]$ 147 Unassigned; illegal.</p>		<p>140. N 0 DEVICE Peripheral 142 FROM LENGTH Transfer Modes on other 141. N 0 DRUMADDR Drum 142 COREADDR LENGTH Transfer side 142 TO 0 Internal 142 FROM LENGTH Transfer 143 (3) Copy z into X to X + Y - 1 (2) Clear to zero X to X + Y - 1 144 Search table $\left[\begin{matrix} w \geq y \text{ (ascending)} \\ w \leq y \text{ (descending)} \end{matrix} \right]$ 145 starting at X $\left[\begin{matrix} w \geq y \\ w \leq y \end{matrix} \right]$ 146 for first $\left[\begin{matrix} w_u = Y_u \text{ or } w_m = 0 \\ \text{and set } z' = \text{address of } w \end{matrix} \right]$ 147 Unassigned; illegal.</p>		<p>140. N 0 DEVICE Peripheral 142 FROM LENGTH Transfer Modes on other 141. N 0 DRUMADDR Drum 142 COREADDR LENGTH Transfer side 142 TO 0 Internal 142 FROM LENGTH Transfer 143 (3) Copy z into X to X + Y - 1 (2) Clear to zero X to X + Y - 1 144 Search table $\left[\begin{matrix} w \geq y \text{ (ascending)} \\ w \leq y \text{ (descending)} \end{matrix} \right]$ 145 starting at X $\left[\begin{matrix} w \geq y \\ w \leq y \end{matrix} \right]$ 146 for first $\left[\begin{matrix} w_u = Y_u \text{ or } w_m = 0 \\ \text{and set } z' = \text{address of } w \end{matrix} \right]$ 147 Unassigned; illegal.</p>		<p>140. N 0 DEVICE Peripheral 142 FROM LENGTH Transfer Modes on other 141. N 0 DRUMADDR Drum 142 COREADDR LENGTH Transfer side 142 TO 0 Internal 142 FROM LENGTH Transfer 143 (3) Copy z into X to X + Y - 1 (2) Clear to zero X to X + Y - 1 144 Search table $\left[\begin{matrix} w \geq y \text{ (ascending)} \\ w \leq y \text{ (descending)} \end{matrix} \right]$ 145 starting at X $\left[\begin{matrix} w \geq y \\ w \leq y \end{matrix} \right]$ 146 for first $\left[\begin{matrix} w_u = Y_u \text{ or } w_m = 0 \\ \text{and set } z' = \text{address of } w \end{matrix} \right]$ 147 Unassigned; illegal.</p>		<p>140. N 0 DEVICE Peripheral 142 FROM LENGTH Transfer Modes on other 141. N 0 DRUMADDR Drum 142 COREADDR LENGTH Transfer side 142 TO 0 Internal 142 FROM LENGTH Transfer 143 (3) Copy z into X to X + Y - 1 (2) Clear to zero X to X + Y - 1 144 Search table $\left[\begin{matrix} w \geq y \text{ (ascending)} \\ w \leq y \text{ (descending)} \end{matrix} \right]$ 145 starting at X $\left[\begin{matrix} w \geq y \\ w \leq y \end{matrix} \right]$ 146 for first $\left[\begin{matrix} w_u = Y_u \text{ or } w_m = 0 \\ \text{and set } z' = \text{address of } w \end{matrix} \right]$ 147 Unassigned; illegal.</p>	
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Note: 3-address forms given. Unless stated otherwise, get 2-address by reading x', x'' for z', z'' and putting $z = 0$.
* Individual notes overleaf.

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MODES IN 140 AND 141

Y denotes Y-address in the 142-instruction

- 40 $z'_1 + (z'_1/y_1) = x_1/y_1; 0 \leq z'_1/y_1 < 1$
- 41 $z'_1 = (x_1/y_1)_r$ or $(x_p/y_p)_r; -\frac{1}{2} \leq (x/y) - z'_1 < \frac{1}{2}$
- 42 $z'_M = (x_1/y_1)_r$ or $(x_p/y_p)_r; -\frac{1}{2} \leq (x/y) - z'_M < \frac{1}{2}$
- 43 $z'_p = (x_p/y_p)_r$ or $(x_1/y_1)_r; -\frac{1}{2} \leq (x/y) - z'_p < \frac{1}{2}$
- 44 $z'_1 + (z'_1/y_1) = x_1/y_1; 0 \leq z'_1/y_1 < 1$
- 45 $z'_p = (x_p/y_p)_r$ or $(x'_M/y_1)_r; -\frac{1}{2} \leq (x/y) - z'_p < \frac{1}{2}$
- 50 to 53 } The } 24 } places shifted take no time
- 54 to 57 } last } 48 } if shift number \geq stated number.
- 75 2-address is recommended unconditional jump.
- 76 2-address: Jump to X if Y = 0
- 77 2-address: Jump to X if Y \neq 0
- 100 $z' = y_1(y_6(\dots(y_1(y_0x + x_0) + x_1) + \dots) + x_7$
 If m.s. } 00 } check that m.s. bit of x_i is 0
 2 bits } 01 (+16) } check m.s. 2 bits of x_i are 01
 of y_i } 10 (+32) } make no check
 are } 11 (+48) } treat x_i as zero
- 101 (3) } x' = characters resulting } z_c } y^* contains radices
 (2) } from conversion of } x_c } and y their product
 To convert } SP }
 non-significant } 0 (digit) } add } 0
 zeros } full stop } } 16
 as } UC } } 32
 } } } 48 } to radix
- 102 $v = 0$ if OVR clear
 $v = \pm 2$ if OVR set, sign of v opposite
 to that of x_p . OVR' = 0 unless z'_0 overflows
- 104 Convert 2-character data in x to 4 characters
 according to code table starting in Y
 (3) $z'_m = z_m, z'_n =$ new characters
 (2) $x'_m = 0, x'_n =$ new characters
- 120 If $\begin{cases} Y \geq 0 \\ Y < 0 \end{cases}$ } $\begin{cases} z'_m = \text{number} \\ \text{of 1-bits in } \end{cases}$ } $\begin{cases} \text{first } \\ \text{last } \end{cases}$ } $\begin{cases} |Y| \text{ bits of } x. z'_s = \text{inverse} \\ \text{of next bit of } x \end{cases}$
- 121 $z' = x$ shifted cyclically right Y bits (Y signed)
 If $|Y| \geq 24$, last 24 places shifted take no time.
- 122 (3) } $x' = y$ shifted } Z } characters.
 (2) } cyclically left } z_c
- 123 (3) } Leave unchanged } Z } characters of x'_L , follow them
 (2) } the first } z_c } by all y , clear rest of x'_L
- 124 (3) If $\begin{cases} Y \geq 0 \\ Y < 0 \end{cases}$ } $\begin{cases} x' = x \\ \text{shifted } \end{cases}$ } $\begin{cases} \text{left} \\ \text{logically right} \end{cases}$ } until $\begin{cases} \text{left-most} \\ \text{right-most} \end{cases}$ } $\begin{cases} \text{1-bit shift} \\ \text{off but noted} \\ \text{more than } | \end{cases}$
 $z' =$ shift number. If no 1-bit removed then $z'_m = |Y|$ and $z'_s = Y|$ places
 (2) $x' =$ shift number, etc.. x and its shifted form overwritten. : 1
- 125 (3) $x'_p = (x_p + v)2^m$ [$x'_p > 0$]; $z'_1 = z_1 - m$; OVR' = 0
 (a) $v = 0$ if OVR clear, $v = \pm 2$ if set (sign opposite
 to that of x). OVR left clear.
 (b) m is an integer such that
 either (i) $\frac{1}{2} \leq x'_p < 1$ and $-1 \leq m \leq Y$
 or (ii) $-1 \leq x'_p < -\frac{1}{2}$ and $-1 \leq m \leq Y$
 or (iii) $-\frac{1}{2} \leq x'_p < \frac{1}{2}$ and $m = Y$
 (c) If $m < 0$, shifting down is unrounded;
 only happens if $v \neq 0$ (i.e. OVR set on entry)
- (2) Illegal.
- 126 (2) $x' + ey' = x + ey + ev; y' \geq 0; \text{OVR}' = 0$
 $v = 0$ if OVR clear, $v = \pm 2$ if set (sign opposite
 to that of y). OVR left clear unless x' overflows
 (3) As (2) but result is $z' + ey' =$ justified form of $x + ey$.

Paper Tape	Magnetic Tape
1 Read 7-tr. up to NL, at most Y chars.	1 Read forward
2 Read 7-tr., Y chars.	2 Read backward
6 Read 5-tr., Y chars.	14 Rewind
16 Disengage	21 Write, long gap
21 Punch 7-tr. up to NL, at most Y chars.	22 Write, short gap
22 Punch 7-tr., Y chars.	28 Erase
28 Punch 5-tr., Y chars.	

Punched Cards	Keronic Printer
1 Read, IBM	16 Disengage
2 Read, ICT	21 Print up to NL, at most Y chars.
4 Read, BULL	22 Print Y chars.
7 Read, IBM and binary	
8 Read, ICT and binary	
11 Read, BULL and binary	
14 Read, binary	
16 Disengage	
19 Read normal and interstage	
21 Fill data buffer, punch (coded)	
22 Fill data & code buffers, punch (binary)	
26 Fill code buffer	

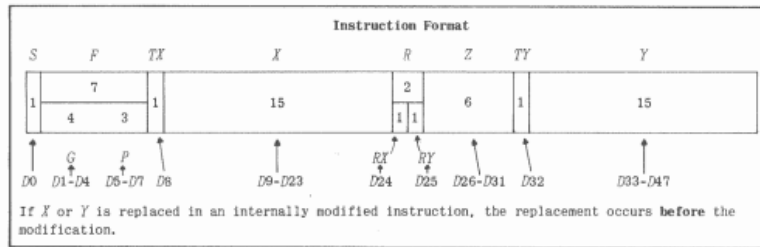
Line Printers
16 Disengage
21 Fill data buffer } with full character set
22 and print a line } with part character set
26 Fill code buffer

Drum	All Devices
1 Read Y words from drum-store	13 Interrogate
21 Write Y words into drum-store	

SOME SPECIAL 150-INSTRUCTIONS

Summary of events associated with the various values of Z in the instruction 150 X Y Z

- 1 Timing flag
- 2 Branch interlock
- 10 Stop (Halt or Suspend)
- 11 Abolish
- 12 Date and time
- 13 Message to Flexowriter
- 14 Question to Flexowriter
- 15 Read Directory
- 20 Set Monitoring style
- 21 Set peripheral incident
- 22 Set Monitoring peripheral
- 23 Return from private Monitoring
- 24 Start New Branch
- 25 Restore Branch Conditions
- 30 Reserve peripheral
- 31 Relinquish peripheral
- 32 Get geographical name
- 33 Load document
- 34 Get document if loaded
- 36 Change name of peripheral
- 40 Read block 0
- 41 Write block 0
- 42 Get current block number
- 43 Write non-sequential block
- 50 Chapter change
- 51 Load chapter of semi-built-in program
- 52 Change drum reservations
- 53 Change core reservations



Pseudo-Registers

The following description is taken from section 2.6.0 of the ORION Programming Manual.

2.6.0

The pseudo-registers are a number of auxiliary registers containing useful constants or the state of switches inside or outside the machine. They can be read from but it is not possible to write to them. They are referred to by the instructions 20-27, 66, 67 and 112 (see sections 3.2, 3.6 and 3.11) - these instructions take the same time as the corresponding instructions (00-07, 60, 61 and 110) for ordinary registers. Pseudo-registers are available to all programs impartially - they are not subject to lockout or reservation checking. The Y^{th} pseudo-register is referred to as PY, and its contents as pY.

2.6.1 Contents of Pseudo-registers

The contents of even-numbered pseudo-registers from P0 to P18 are given below; for odd number registers $p(2n+1) = \neg p(2n)$, i.e. the contents of each odd numbered pseudo-register is the inverse of the contents of the preceding even numbered register.

p0 = 0

p2 = Local civil time - see section 2.6.3 for details of the code.

p4 = Zero if overflow clear, all ones if overflow set.

Any instruction referring to p4 or p5 clears overflow.

p6 is as p4 except it is not cleared when used.

p8 = upper half word mask - i.e. 24 ones followed by 24 zeros.

p10 = -1.0 i.e. one followed by 47 zeros.

p12 = $\frac{1}{2}$, i.e. a zero, a one followed by 46 zeros.

p14 = Mask for X address, i.e. 9 zeros, 15 ones, 24 zeros.

p16 = Mask for Z address, i.e. 26 zeros, 6 ones, 16 zeros.

p18 = Handswitches. The handswitches are a set of 48 keys which are provided for the use of the engineers; their use by programmers is not recommended except in very special circumstances - e.g. Pegasus simulator. It is the operator's responsibility to ensure that only one program using the handswitches is in the machine at once.

2.6.2 Unallocated Pseudo-Registers

At present pseudo-registers 20-31 inclusive contain zero for even numbers and all ones for odd numbers. Pseudo-register numbers above 31 are taken modulo 32, i.e. only the least significant five bits are decoded. Programmers are strongly recommended not to use either of these facts as they may be changed if it is decided to add further pseudo-registers to the machine.

2.6.3 Local Civil Time

The digital clock in Orion is a 24-hour clock in hours, minutes and seconds. It is stored in a one out of n code, i.e. in each field which has n possible values one and only one of n bits is a 1. In each case the m.s. bit of the field represents 0, the next 1, the next 2 and so on. The fields are as follows:

D0 to D2 tens of hours
D3 to D12 hours
D13 to D18 tens of minutes
D19 to D28 minutes
D29 to D34 tens of seconds
D35 to D44 seconds
D45 to D47 not used (always zero)

e.g. the time 17.08.23 is represented by 1-bits in digits:

1, 10, 13, 27, 31, 38

and 0-bits elsewhere.

Third Character (Twelves of Hours)			Fourth Character (Hours)		
Value	Binary Code	Decimal Code	Value	Binary Code	Decimal Code
0	000000	0	0	000000	0
1	000001	1	1	000001	1
			2	000011	3
			3	000010	2
			4	000110	6
			5	000111	7
			6	001111	15
			7	001110	14
			8	001010	10
			9	001011	11
			10	001001	9

11	001000	8
0	001000	8
1	001001	9
2	001011	11
3	001010	10
4	001110	14
5	001111	15
6	000111	7
7	000110	6
8	000010	2
9	000011	3
10	000001	1
11	000000	0

Fifth Character
(Tens of Minutes)

Sixth Character
(Minutes)

Seventh Character
(Tens of Seconds)

Eighth Character
(Seconds)

Value	Binary Code	Decimal Code
0	000000	0
1	000001	1
2	000011	3
3	000111	7
4	000101	5
5	000100	4
0	000100	4
1	000101	5
2	000111	7
3	000011	3
4	000001	1
5	000000	0

Value	Binary Code	Decimal Code
0	000000	0
1	000001	1
2	000011	3
3	000111	7
4	000101	5
5	001101	13
6	001111	15
7	001011	11
8	001001	9
9	001000	8
0	001000	8
1	001001	9
2	001011	11
3	001111	15
4	001101	13
5	000101	5
6	000111	7
7	000011	3
8	000001	1
9	000000	0