

Version 3 January 2005

Ferranti Mercury.

X2. Systems Architecture.

Note:- Ferranti terminology is used with modern equivalents in brackets when first used.

Index

B1 Computer and user features

D4 Hardware and technical details

References

B1 Computer and User features.

According to the manufacturer's literature¹ the Ferranti Mercury Computer was a **high speed** machine using **hardware floating point arithmetic** and with **exceptionally large storage capacity**. The main applications areas were foreseen as in science and technology, with nine areas listed as:-

volume computation	matrix algebra	X-ray analysis
Eigenvalue problems	design optimisation	linear programming
stress analysis	relaxation techniques	partial differential equations.

“When an IBM representative, Samuels, visited Dover Street and saw the electronic floating point in operation he was very impressed. IBM stopped production of their current machine soon after and came out later with a floating point version.”

(DBG Edwards, private communication)

Mercury was unusual in that it was designed for floating point use exclusively. The integer arithmetic was limited to 10 digits (bits) and thus is difficult to compare with other machines on the basis of fixed point operations. The multiplier was a parallel/serial design, operating on 10 digits in parallel with three serial sections using what later became known as carry save adders. Two multiplier bits were decoded per cycle (Mark I performed 20 digits in parallel in two sections, ‘decoding’ one digit at a time and also using the ‘carry save’ technique).

D4 Hardware Technical Details.

The **CPU** was serial in operation, with a clock speed of 1 Mc/s (Mhz). The computational store (below) had a read time of 10 μ S so was read 10 bits in parallel. Arithmetic was basically in floating point form with a 10-digit (bit) exponent and 30 digit argument (mantissa, characteristic). Registers were constructed of electromagnetic delay lines except for a small number of staticised ones (memory address, function) and gates etc used semiconductor diodes and thermionic pentode valves (6CH6)³.

Instruction times: Floating point add = 180 μ S; multiply = 300 μ S;
division (by subroutine) = 3.5 mS;
‘Short orders’ including 10-digit ‘B’ add = 60 μ S (no B multiply).

The store consisted of two parts. The **Computational Store**² (main store) was magnetic cores arranged as two planes of 1K cores on either side of a plate and with 20 plates in four groups of five. This gave 1K words of 40 digits. A parity digit was provided for each 10 digits. Addressing was as 1K words which could be medium words of 20 digits (only half the store) or long words of 40 digits. Ten digits (+ parity) were read in parallel - one group as noted above. The second (third and fourth) half words were read automatically. Half words (10 digits) were also addressable in the first half of the store.

The **Main Store** (backing store, drum) was on four or eight drums each containing 4K words of 40 digits, again with parity for each 10 digits. Drums were arranged in sectors of 128 10-digit words. There were two sectors per track and 64 tracks per drum. Thus the

Version 3 January 2005

'exceptionally large store' consisted of 16K long words of 40 digits (80K bytes) plus the 5K bytes in the computational store (4-drum version). Drum speed was 3472 rpm giving a revolution time of 17 mS. One half word could be read per 60 μS short order giving a maximum transfer time for a single block of 25 mS. Transfers were done a sector at a time and it was possible to transfer consecutive sectors to save on latency time.

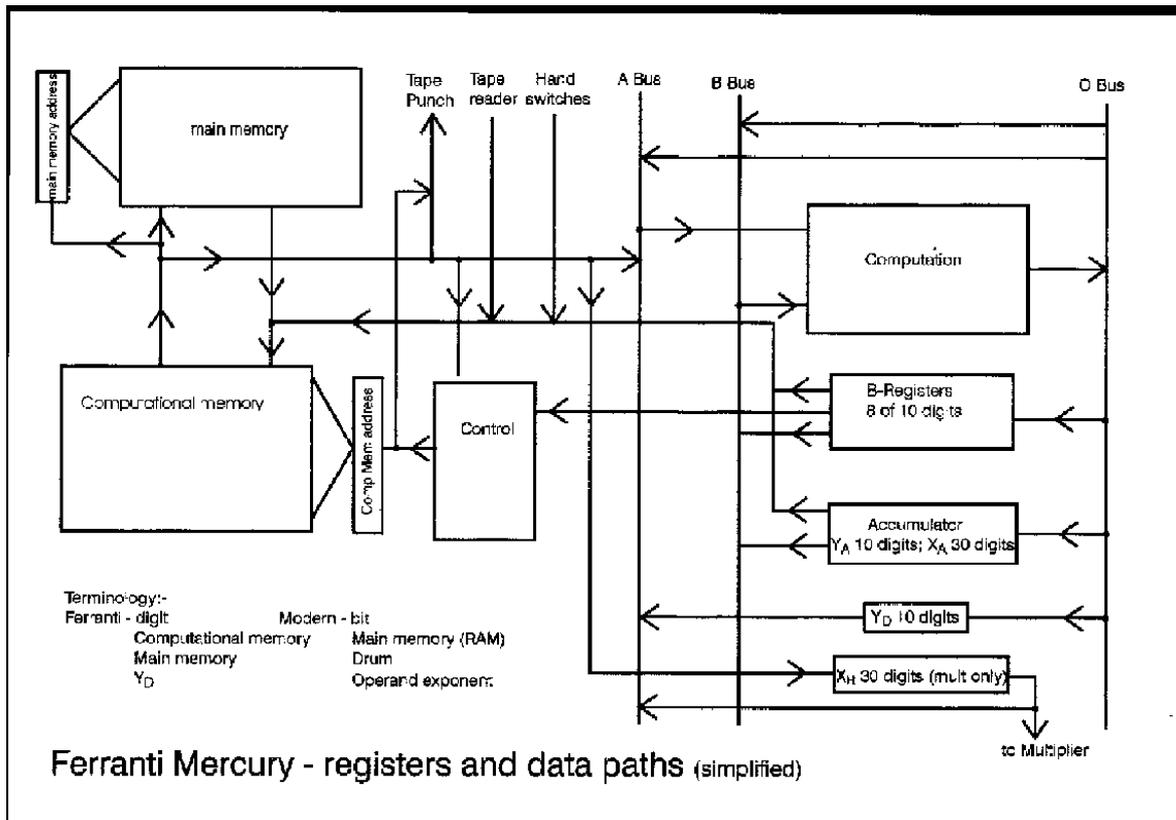
Input to the machine was by high speed paper tape reader at 200 characters per second (5 bit). **Output** was via a 33 character per second paper tape punch which could then be **printed** on a teleprinter at seven characters per second. Later, punched card, magnetic tape and a line printer became available.

Word length: 40 digits plus one parity per 10 digits.

Data representation: Floating point numbers 'mainly' as 10 digit exponent and 30 digit argument. Range of numbers was 2^{-256} to 2^{255} (approx. 10^{-78} to 10^{78}) positive and negative. The argument was in true complement form in the range -1 to $< -\frac{1}{2}$; $\frac{1}{2}$ to < 1 .

Instruction length: 20 digit 'medium' word consisting of 10 digit function and 10 digit address. Most instructions were B-modifiable.

Character length: 5 digits which can be packed two per half word.



D3 References

¹ *Description of the Ferranti Mercury Computer*. Ferranti List DC 30, June 1957; MSIM reference F2 Series 6 Box 13.29.

² *Ferranti Mercury Computer - Recommended Terminology*. List CS 205, July 1958; MSIM reference F2 Series 6 Box 4/13.

³ SH Lavington; *History of Manchester Computers*. NCC Publications, 1975.

Other useful references.

Ferranti Mercury Computer - Questions and Answers; List CS 120a, August 1957; MSIM reference F2 Series 6 Box 4/5. Contains summary of facilities and requirements, including weights, sizes, power and cooling requirements as well as technical details etc. etc..

K Lonsdale, ET Warburton; *Mercury; A High Speed Digital Computer*. Proc IEE Vol 103 Suppl. 2 pp 174 - 183.

T Kilburn, DBG Edwards, GE Thomas; *The Manchester University Mark II Digital Computer*. Proc IEE Vol 103 Suppl. B pp 247 - 268 (MEG; see Lonsdale and Warburton for differences in Mercury).

DBG Edwards; *Design and Construction of an experimental High Speed Digital Computer*. PhD Thesis, University of Manchester, 1954 (MEG).

GE Thomas; *The Design of an Electronic Digital Computer*. PhD Thesis, University of Manchester, 1954. (Also MEG. The main thesis is just over 100 pages and appears very clear. The appendices are another 100+ pages and are a mine of useful information. Includes a full diagram of the computational unit including the B-registers. Also details of the components used including valves, semiconductor diodes with their characteristics, resistors, capacitors, and delay lines (including winding details).)